A Low SWaP-C prototype Ka-band Frequency Synthesizer for Atomic Clocks

Michael O. Toennies*, Lin Yi†, Eric A. Burt and Robert L. Tjoelker
Jet Propulsion Laboratory, California Institute of Technology
Pasadena, California, 91109, U.S.A.

***Abstract* – We present a low size, weight, power and cost (SWaP-C) prototype circuit of a Ka-band frequency synthesizer. It takes advantage of a phase-locked loop single integrated circuit (IC) and harmonic generation with high speed CMOS gates. We use a direct digital synthesizer (DDS) IC to tune the final output with micro-Hertz resolution. An ultra-low-power micro controller that could serve as the clock controller is used to control the PLL and the DDS. All components are commercial off the shelf (COTS) with acceptable industrial support. The total power consumption is about 1.6 Watt with -45 dBm useful output at 40.507347996 GHz. The short-term instability introduced by the prototype is 7.3E-14 at 1s. The prototyped subsystem uses COTS demonstration boards for the sake of agile prototyping. There is still significant margin for improvement of the size and weight.**

Keywords – atomic clock, frequency synthesizer, low power

I. INTRODUCTION

Low phase noise frequency synthesis is a critical subsystem in atomic clock architectures. It transfers the frequency stability from the local oscillator radio frequency to the microwave atomic clock transition. For the mercury trapped ion clocks [2][3] developed at NASA's Jet Propulsion Laboratory, the Ka-band Hg+ clock transition frequency is 40.507347996 GHz. This presents a significant challenge for low SWaP-C applications due to the high frequency, bulky and expensive discrete microwave components with limited availability, and stringent phase noise requirements of the atomic clock system. Previous ground-based versions of trapped ion atomic clocks have used frequency synthesis schemes based on a step recovery diode (SRD), which produces exceptional phase noise, but uses significant power. Developing a low phase noise frequency synthesizer with lower cost and power is needed for future trapped ion clock implementations.

II. SYSTEM OVERVIEW

A basic system diagram of our CMOS frequency synthesis scheme is shown in Fig. 1. The input frequency is 100 MHz supplied by an on-site hydrogen maser. This signal is then sent as an input to both the Analog Devices AD9956 Direct Digital Synthesizer (DDS) and an Analog Devices ADF4108 phase locked oscillator (PLO) component, which is an integrated union of a phase-locked loop (PLL) and a voltage-controlled oscillator (VCO). For simplicity and rapid prototyping, a demo board for this PLO was utilized, which bounded the particular output frequency we could use and we believe resulted in a higher phase noise than is possible with this architecture. Redesigning this PLO to use tuned feedback filters with the explicit intention of being used for this application would probably improve performance. Both the DDS and PLO are controlled via a Texas Instruments MSP432 microcontroller using the SPI protocol to control the operation on one data bus. Finally, the desired output frequencies, which in this trial were 5.785 GHz for the PLO and 12.347996 MHz for the DDS, are mixed together in a CMOS gate Hittite Semiconductor HMC844LC4B.

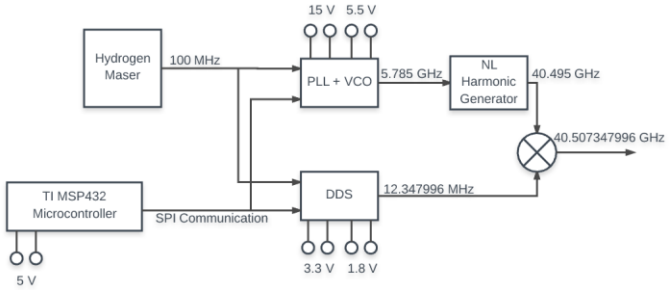

Fig. 1. Signal flow diagram for frequency synthesizer

III. MEASUREMENT OVERVIEW

Both power consumption and frequency stability were recorded for this setup. Power consumption was measured via simple DC power monitoring for each of the units independently, excluding the hydrogen maser.

Frequency stability was measured both via recording phase noise and calculating the Allan Deviation. For both of these measurements, the main signal was first down-converted to 300 MHz via an RF mixer and an external signal provided by an Agilent E8257D signal generator, and then down-converted further to 100 MHz. From this point however, the phase noise results were obtained differently depending on whether the output spectrum had nearby frequency components or not. If the output spectrum had only one spur of significant amplitude within roughly a 300 MHz bandwidth, then a simple down-conversion from the target frequency to 100 MHz was sufficient, with the final signal sent to an HP5125A phase noise analyzer. However, if the final stage CMOS gate was included as part of the device under test, numerous frequency components will exist in the output

* 2017 JPL Summer Internship Awardee, current affiliation: The Boeing Company, RF Products, El Segundo CA, USA
† Email: Lin.Yi@jpl.nasa.gov

spectrum and be spaced apart by roughly 12 MHz. Since the HP5125A is unable to filter out input components that are within ~300 MHz from the input frequency, a new phase noise measurement system was needed.

The alternative method of measuring phase noise sends the target frequency, once down-converted to 100 MHz, to a 100 MHz cleanup loop to remove all frequency components that are not equal to 100 MHz. Finally, the error signal between the internal reference oscillator and the down-converted target frequency is sent to a HP3561A Dynamic Signal Analyzer. Phase noise can thus be recorded for this output signal with mixer components. It should be noted here that the phase noise of the oscillator internal to the 100 MHz cleanup loop did contribute to the final phase noise measurement, but based on noise floor measurements was not a significant fraction of measured results. A system diagram of this alternative phase noise analyzer is included below in Fig. 2. For both Allan Deviation and phase noise measurements, the noise floor was defined as using identical down-conversion components, and replacing the original synthesizer with an Agilent E8257D signal generator.

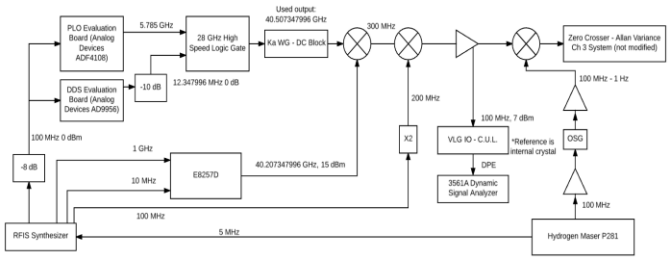

Fig. 2. Diagram of final synthesizer's phase noise testing system

IV. RESULTS

The total power consumption of the synthesizer is found in Table. 1 to be ~1.5 W. There is still potential to reduce the power. One way to do this is to choose a low power DDS with a shorter tuning-word compatible with the stability requirement. Another way is to choose a low power VCO in the PLO. The mid- and long-term Allan Deviation results for this synthesizer are included in Fig. 3. Long-term in this context is defined as exceeding 1000 seconds. Fig. 4 shows the phase noise of the synthesizer at ambient temperature. A peak output signal strength of -47 dBm was recorded using the COTS components listed above. For reference, a signal strength between -50 and -40 dBm is required to be successfully used in a trapped-ion clock.

Circuit Board	Power Supply Voltage	Power Consumption
DDS	+3.3 V	0.162 W (49 mA)
	+1.8 V	0.124 W (69 mA)
MSP432	+3.3 V	0.009 W
45 Gb/s Logic Gate	-3.3 V	0.475 W (144 mA)
PLO	+5.5 V	0.792 W (144 mA)
Total		1.562 W

Table. 1. Power consumption for each included COTS circuit boards, as well as the total system power consumption – DC power used to generate the 100 MHz reference signal is not included

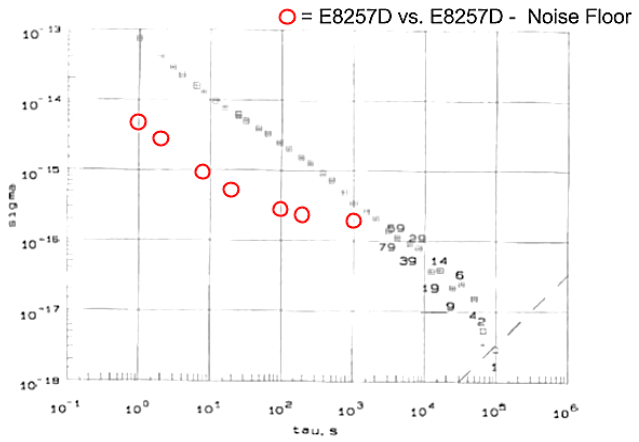

Fig. 3. Allan Deviation plot for final synthesizer operating at Ka-band. Red circles indicate the Allan Deviation of the noise floor for this setup.

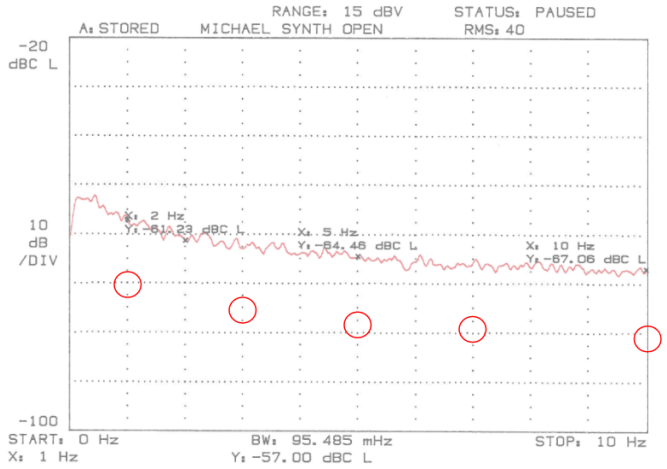

Fig. 4. Phase noise for final synthesizer with ambient temperature (25° C). Red circles indicate phase noise measured for noise floor, or with Agilent E8257D providing main signal.

V. CONCLUSION

After assembling a prototype module using various COTS components, a low-power Ka-band synthesizer for use as a RF probe for an atomic clock was successfully created. Its signal strength was sufficient for atomic clock applications. While these results were deemed sufficient, given the nature of this assembly, it is very likely that better performance is possible even without developing a single integrated synthesizer using this technique, in particular by improving upon the PLO's demo board performance.

Given the prototype nature of this setup, prudent next steps would include more rigorous temperature sensitivity testing, which if successful, could lead to an increasingly integrated setup for enhanced robustness.

ACKNOWLEDGEMENT

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the

National Aeronautics and Space Administration. Copyright 2018 California Institute of Technology. Government sponsorship acknowledged. We sincerely thank W. Diener, A. Kirk, B. Tucker for the technical support and discussion during this work.

REFERENCES

[1] Tjoelker, R.L., Prestage, J.D., Burt, E.A., Chen, P., Chong, Y.J., Chung, S.K., Diener, W., Ely, T., Enzer, D.G., Mojaradi, H. and Okino, C., “Mercury ion clock for a NASA technology demonstration mission.” *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, *63*(7), pp.1034-1043 (2016).

[2] Tjoelker, R.L., Burt, E.A., Chung, S., Hamell, R.L., Prestage, J.D., Tucker, B., Cash, P. and Lutwak, R., "Mercury atomic frequency standards for space based navigation and time-keeping." *Proceedings of the 43rd Annual Precise Time and Time Interval Systems and Applications Meeting, Long Beach, California*. 2011.

[3] Burt, E.A., Yi, L., Tucker, B., Hamell, R. and Tjoelker, R.L., “JPL ultrastable trapped ion atomic frequency standards.” *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, *63*(7), pp.1013-1021 (2016).